REMARKS

Claims 1 and 3-7 are all the claims pending in the application. Claim 2 is canceled. Claims 1, 3 and 4 are amended.

Applicants note that the amendment made to claim 1 simply places claim 2 into independent form, and that the amendment should be entered in order to place the application in condition for allowance for the reasons given subsequently or to place the application in better condition for appeal. No new issues are raised and no new search is required.

Claim Rejections - 35 U.S.C. § 103

Claims 1-7 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Cabler (5,625,357) in view of Ledzius et al (5,323,157). Applicants respectfully traverse this rejection for at least the following reasons.

At pages 3-5 of the Office Action, the Examiner repeats the text of the previous Office Action with regard to the basis for rejection of claims 1-7 as being unpatentable over Cabler (5,625,357) in view of Ledzius et al (5,323,157). At page 2 of the Office Action, in the Response to Arguments section, the Examiner addresses the several arguments for patentability raised in the previous Amendment of August 14, 2006.

As already noted, Applicants now have placed rejected claim 2 into independent form by inserting its limitations into claim 1. Claim 1, as now stated, is distinguishable over the prior art for several reasons, including those previously given and the recitation of "a full differential operational amplifier" within the claimed output filter for a delta sigma modulator. As explained

subsequently, this feature is an important advance. Neither Cabler nor Ledius discloses this feature.

Cabler

No Full Differential Operational Amplifier

Cabler does not disclose that the elements 25 and 27 of Fig. 4 each are "a full differential operational amplifier". Accordingly, "a full differential operational amplifier" does not appear in Cabler, and there is no disclosure of the feature of amended claim 1 in Cabler, namely, Cabler does not at all disclose "a full differential operational amplifier". The configuration of Cabler requires (1) two amplifiers 25 and (2) the amplifier 27 for receiving the outputs of the amplifiers 25. Thus, the circuit must be significantly larger-scale than that of the present invention. Further, according to the present invention, since the outputs from the FIR 4 are differentially inputted to the full differential operational amplifier 6a, the common mode noises can be removed efficiently.

No Two Constant Current Sources

In addition to this clear distinction, Applicant again submits that Cabler fails to teach two constant current sources. The Examiner points to Fig. 1 of Cabler and asserts that the FIR (50) comprises two sources I_0 and I_1. Applicants admitted that the Examiner is correct with regard to Fig. 1 of Cabler. The Examiner also notes Applicants' argument that there is only one current source I_{REF} illustrated in the remaining Figures of Cabler. Applicants argued that the use of only one current source is a key feature of the embodiments illustrated in Figs. 2, 3 and 5A-5C.

Applicants also argued that these figures illustrate two current paths that are directed through two resistances R_0 and R_1 and carry different currents, I_0 and I_1, but there is only one

current source. Thus, Applicants argued that only the teachings of Fig. 1 in Cabler with respect to the remaining limitations in the claim need be considered.

In reply, the Examiner simply states "Applicant is reminded that the Examiner is free to consider any drawing of the patent which she/he deems to be relevant.

Applicants would not disagree, and wishes to clarify that the relevant teachings in Cabler are in Fig. 1. There, the Sigma-delta 16 provides plural control bits B_0-B_N on line 12 to shift register 14. The shift register 14 provides "N" outputs B_0, B_1, B_2 etc., as explained at col. 1, lines 38-54. As is seen in Fig. 1, there is one current source for **each** shift register output, as is clear from the outputs B_0, B_1, B_2 etc. and the corresponding current sources I_0, I_1, etc. Similarly, there is a corresponding non-inverted switch B_0, B_1 etc. and inverted switch B0, B_1, etc for each current switch.

Applicants again emphasize that the circuit in Cabler requires **more than two** current sources and more than two dedicated pairs of inverted and non-inverted switches, one for each bit B_0-B_N. All of the outputs from the non-inverted switches B0-B_N flow to non-inverted output 62 and all of the outputs from the inverted switches B0-B_N will flow to inverted output 58. In addressing this difference, the Examiner simply states that "Cabler does teach in figure (1) two current sources and the applicant claims two current sources." However, the use of two current sources alone is not the invention, it is an invention in the context of the structure of the claimed circuit where there are more than two transistor circuits. Applicants respectfully submit that this has not been addressed by the examiner and must be considered.

Specifically, the Examiner has not challenged Applicants' observation that the present invention uses only two constant current sources, one for the non-inverted line and one for the

inverted line into the differential amplifier of current to voltage circuit 6. Each current source is coupled to a plurality of MOS transistor circuits (T1-Tn), each MOS transistor circuit having a pair of inverted and non-inverted outputs. This arrangement has the advantage of reduced components and simplified circuitry.

Even more specifically, the Examiner has not addressed the added limitations to the claims that emphasizes that there are only two constant current sources and that more than two switches control such currents. Claim 1 expressly states that there are "n" elements (where n is a whole number **greater than 2**). This limitation is taught in Fig. 1 of the present application, where switches T_1, T_2 - T_n are illustrated. The limitation is not seen in Cabler. Thus, this expressly recited feature is a basis of patentable distinction over the structure of Cabler.

Ledzius

Applicants submit that Ledzius does not remedy these two deficiencies in Cabler, and does not provide a basis for attaining the small scale design of the present invention.

First, as to the limitation of a "full differential amplifier," this feature is not taught in Ledzius. The amplifier 101 connected to the current sources 91 to 93 of Fig. 3 is neither "a full differential operational amplifier" nor "differential input", so that it does not fulfill the effect of the present invention as mentioned above.

Second, as to the use of two current sources, Ledzius does not teach how to modify Cabler to have this feature.

Ledzius is cited merely for its teaching in Fig. 3 of a sigma delta DAC including a plurality of flip-flops (81-83) used as delay elements, each flip flop having two outputs, each coupled to a respective one MOS transistor, as illustrated in Fig. 4. The teaching in Ledzius of

plural current sources for respective flip flops, as illustrated in Fig. 3, would not teach or suggest the structure, as now claimed.

Conclusion

Applicants respectfully submit that the prior art references do not teach an output filter for a delta sigma modulator that comprises:

(1) first and second constant current source [8a, 8b], and

(2) a FIR filter [4], where the FIR filter recited in the claim has

(a) a plurality of delay elements [F_1-Fn] arranged in cascade, where n is a whole number greater than two, and where

(b) each element is operative to output data from the delta sigma modulator [2] by controlling currents via n switches from the constant current source on the basis of each of the output data.

Also, there is no generation of a plurality of weighted currents, which are weighted according to a filter characteristic, where the weighted currents are added and outputted in an output side of the FIR filter.

Finally, there is no "full differential amplifier," as now claimed.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

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